Progress Report

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Self-Checking State Machine Realization in CMOS

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In this reporting period, we have studied the currently available techniques for designing totally self-checking checkers for m-out-of-n codes. Such codes can be used for state assignment in self-checking state machines. The major advantage of m-out-of-n codes is that they can detect single and unidirectional multibit errors in the encoded information bits. Thus, if a circuit is designed such that its output forms an m-out-of-n code, any fault in the circuit which creates a single bit error or unidirectional multibit error at the output can be detected on-line. On-line error detection, also known as self-checking , can be accomplished by using a checker to monitor the circuit output. The output of the checker is 01 or 10 if there is no fault in the circuit under test or in the checker itself, otherwise the output will be 00 or 11.

Several techniques for gate-level design of self-checking checkers have been proposed over the years. Almost all of these consider checker design at the gate-level, and assume the presence of only single stuck-at faults in a checker. Since the checkers are part of self-checking circuits which are likely to be included in VLSI chips, efficient techniques for checker design at the transistor-level must be considered. Also, it is now generally accepted that all faults at the transistor level cannot be modeled as stuck-at faults. Therefore, design techniques for transistor-level implementation of self-checking checkers must be developed.

We have started work on the design of totally self-checking (TSC) checker for k-out-of-2k codes, which are a subset of m-out-of 2m codes. Initially we will design a checker for the 2-out-of-4 code at the transistor level. This checker will be TSC for the following fault set:

i) stuck-at fault at input and output signal lines
ii) stuck-on and stuck-open transistor faults
iii) breaks in input signal lines
iv) bridges between input signal lines

The technique for gate -level implementation of the 2-out-of-4 code is well-known. The traditional approach for obtaining transistor-level implementation of TSC checkers for such codes is to replace each gate in the gate-level implementation, with the equivalent transistor implementation of the gate. We are considering implementation of conventional gates using pass transistors. Preliminary results show that the detection of transistor stuck-open faults are considerably simplified in such structures.

Once a transistor-level TSC checker for the 2-out-of-4 code has been designed, we intend to use it as a building block for implementing checkers for k-out-of-2k code (with arbitrary values of k). We will develop a general procedure for this purpose.

We have also started working on the design of a self-checking checker for Berger code. This code has similar features as the m-out-of-n code but requires least number of check bits among all separable codes.